

Low Density Parity Check Codes for Magnetic Recording Channels

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Abstract—We propose a system for magnetic recording, using a low density parity check (LDPC) code as the error-correcting-code, in conjunction with a rate 16/17 quasi-maximum-transition-run channel code and a modified E²PR4-equalized channel. Iterative decoding between the partial response channel and the LDPC code is performed. Simulations show that this system can achieve a 5.9 dB gain over uncoded EPR4. The algorithms used to design this LDPC code are also discussed.

Index Terms—Iterative decoding, low density parity check codes, magnetic recording.

I. INTRODUCTION

TURBO decoding for magnetic recording channels has been investigated in two different ways: i) using a classical turbo code with at least two component codes [1], [2]; or ii) using a single convolutional code serially concatenated with a partial response (PR) channel which plays the role of a second constituent code of rate one [3]. Both systems perform significantly better than uncoded systems.

In this paper, instead of using a single weak convolutional code, we investigate the use of a powerful block code, namely a low density parity check (LDPC) code [4]–[6], and its iterative decoding with an efficient decoding algorithm.

The paper is organized as follows. In Section II we describe the background of serially concatenated systems and LDPC codes. In Section III we describe a practical LDPC system with turbo equalization for magnetic recording. In Section IV we present the simulation results for the proposed system. In Section V we discuss the design of the LDPC code. Conclusions are given in Section VI.

II. BACKGROUND

A turbo code usually consists of two or more parallel concatenated convolutional codes [7]. The application of turbo codes to magnetic recording channels has the potential for large performance gains over uncoded systems [1], [2]. Turbo equalization is performed by feeding the information from the turbo decoder back to the channel decoder.

Souvignier *et al.*'s serial concatenation scheme simplifies the full turbo system by replacing the turbo code with a single convolutional code [3], and is shown to have about the same performance as the full turbo system, with less complexity.

LDPC codes can be specified by a sparse parity check matrix \mathbf{H} [4]–[6]. The belief propagation (BP) algorithm can be used for soft decoding [4]. It has been shown that the BP algorithm and the turbo decoding algorithm are essentially the same algorithm [8]. By representing the probabilities in log-likelihood ratio (LLR) form, the BP algorithm may be expressed in the logarithmic domain [4], and is referred to as the Log-BP algorithm.

Each row of \mathbf{H} is referred to as a check. The set of bits participating in check m is denoted by $N(m) = \{n: H_{mn} = 1\}$. The set of checks that bit n participates is denoted by $M(n) = \{m: H_{mn} = 1\}$. The Log-BP algorithm is outlined below using the notation of [5].

Suppose a codeword $\mathbf{x} = [x_1, x_2, \dots]$ is transmitted through an AWGN channel with symbols $+1$ and -1 . The received channel vector is $\mathbf{y} = [y_1, y_2, \dots]$. Define $\alpha_n \beta_n = \log[P(x_n = 1|y_n)/P(x_n = 0|y_n)]$, where α_n is the sign and β_n is the absolute value. Similar definitions are used in the following, where the first variable indicates the sign of a real value and the second variable is its absolute value.

Initialization: $\alpha_{mn} \beta_{mn} = \alpha_n \beta_n$ for all m and n .

Iteration:

$$\eta_{mn} \lambda_{mn} = \left(\prod_{n' \in N(m) \setminus n} \alpha_{mn'} \right) \cdot \left(f \left[\sum_{n' \in N(m) \setminus n} f(\beta_{mn'}) \right] \right). \quad (1)$$

$$\alpha_{mn} \beta_{mn} = \alpha_n \beta_n + \sum_{m' \in M(n) \setminus m} \eta_{m'n} \lambda_{m'n}, \quad (2)$$

where $f(\beta) = \log[(1 + e^{-\beta})/(1 - e^{-\beta})]$.

Pseudo-posteriori LLR:

$$\alpha'_n \beta'_n = \alpha_n \beta_n + \sum_{m \in M(n)} \eta_{mn} \lambda_{mn}. \quad (3)$$

Hard decision: $\hat{x}_n = 1$ if $\alpha'_n = 1$.

III. MAGNETIC RECORDING SYSTEMS WITH LDPC CODES

A practical magnetic recording system using an LDPC code is shown in Fig. 1. The proposed system is based on a modified extended E²PR4 (ME²PR4) channel with $h(D) = 5 + 4D - 3D^2 - 4D^3 - 2D^4$ [9].

On the recording end, the user data block is encoded by a rate 16/17 quasi-maximum-transition-run (QMTR) code [9], and then further encoded by an LDPC code. The sequence

Manuscript received February 15, 2000; revised May 15, 2000.

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Publisher Item Identifier S 0018-9464(00)08404-1.

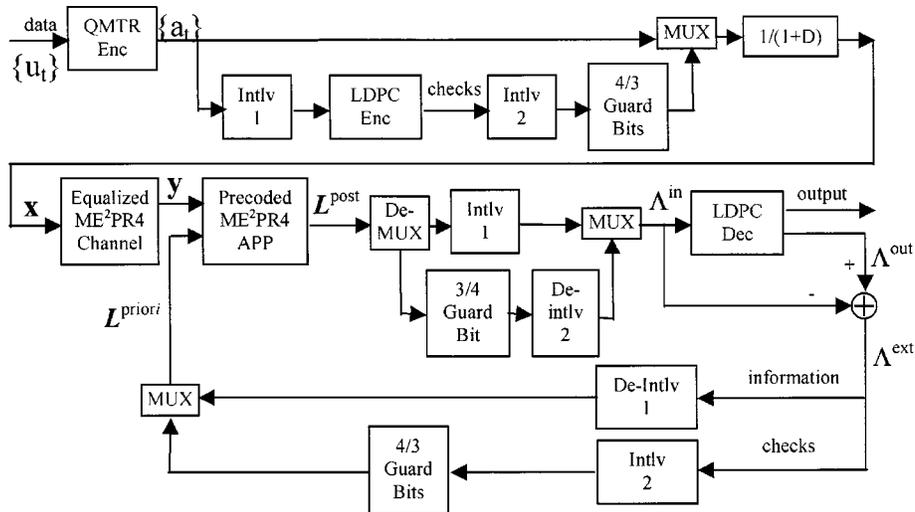


Fig. 1. Block diagram of a PR channel with an LDPC code.

of LDPC check bits is inserted with guard bits so that the run-length conditions are satisfied. On the reading end, an *a posteriori* probability (APP) decoder [10], [11] matches the precoded ME^2PR4 channel. The APP decoder takes \mathbf{y} and the *a priori* LLR L_n^{priori} , and computes the *a posteriori* LLR

$$L_n^{post} = \log[P(x_n = 1|\mathbf{y}, \mathbf{L}^{priori})/P(x_n = 0|\mathbf{y}, \mathbf{L}^{priori})].$$

The LDPC decoder takes the *a posteriori* LLR of the channel decoder as input $\alpha\beta$ in (1), and outputs the *pseudo-posteriori* LLR in (3). The extrinsic LLR $\Lambda^{ext} = \Lambda^{out} - \Lambda^{in}$ is fed back to the channel APP decoder as the *a priori* LLR.

The decoding process has two iteration loops. One is the LDPC loop within the LDPC decoder. After each iteration of LDPC decoding, the decoder checks the syndrome $\mathbf{H}\hat{\mathbf{x}}$. If a valid codeword is found, the LDPC decoding is finished, and the whole decoding process stops. The other iteration loop is the channel loop. It is the turbo equalization between the PR channel and the LDPC code [12]. The channel loop iteration takes place only when the maximum number of LDPC loop iterations is reached without finding a valid codeword.

IV. SIMULATION RESULTS

In our simulation, the Lorentzian channel with isolated pulse $1/(1 + (2t/pw_{50})^2)$ is assumed. User density is defined as pw_{50}/T , where T is the user bit duration. All simulations are performed at user density 2.8. The channel is equalized to the ME^2PR4 channel response, and additive white Gaussian noise with variance σ^2 is assumed before the equalizer. The signal-to-noise ratio (SNR) is proportional to the ratio of the amplitude of the isolated pulse and σ .

We investigate two LDPC codes. LDPC1 is a rate 0.9358 code with block length 4376 given in [13], with column weight 3. We designed LDPC2, with rate 0.9402, 4352 information bits, also with column weight 3. The code was constructed using the method discussed in Section V.

The proposed system with LDPC2 has overall code rate 0.8674 and user block size 4096 bits, whereas the system with LDPC1 has code rate 0.8622 and user block size 3854 bits. In

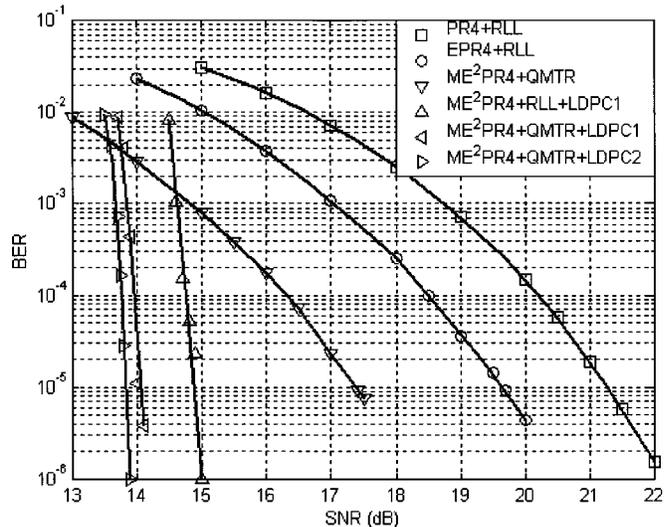


Fig. 2. Performance of LDPC codes on PR channels.

Fig. 1, the maximum number of iterations is set at 50 and 100 for the LDPC and channel iterations, respectively. Simulation results are presented in Fig. 2. Also plotted in the figure are the performance of the rate 16/17 run-length-limited (RLL) coded PR4 channel, the RLL coded EPR4 channel, the QMTR coded ME^2PR4 channel, and the LDPC1 and QMTR coded ME^2PR4 channel.

The simulation results show that our proposed system achieved a 7.5 dB gain over uncoded PR4 or a 5.9 dB gain over uncoded EPR4 at bit error rate 10^{-5} .

The decoding of the LDPC codes has a particularly nice property. The whole decoding process stops if a valid LDPC codeword is found, or if the maximum number of channel iterations is reached without finding a valid codeword. This provides a natural stopping criterion for the iterative decoding as well as a flag indicating that a particular block contains errors, which is a distinct advantage over systems using convolutional codes. An undetected error occurs when a valid LDPC codeword different from the correct one is obtained by the LDPC decoder.

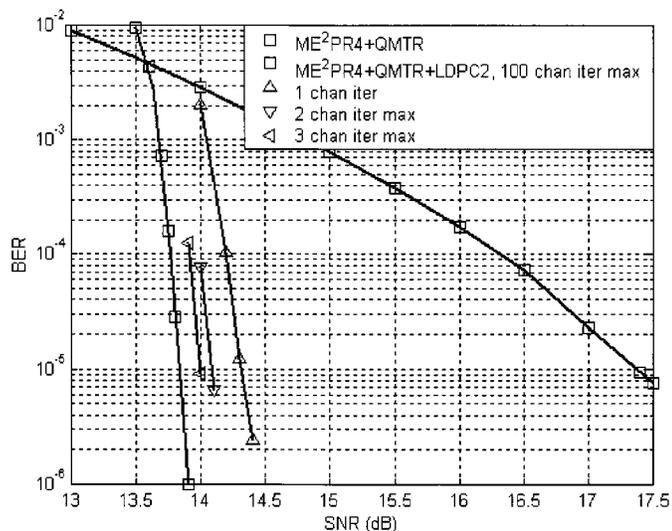


Fig. 3. Performance of the proposed system with few channel iterations.

Throughout our simulation, no undetected errors were observed. This may be due to the large minimum distance of the LDPC codes.

The impact of the maximum number of channel iterations was investigated. Fig. 3 shows the performance of the LDPC2 coded system with 1, 2, 3 and 100 maximum channel iterations. Compared with 100 maximum channel iterations, the performance degradation is about 0.5 dB if no turbo equalization is allowed.

The total number of LDPC iterations for a block is the sum of LDPC iterations in each channel iteration. At bit error rate 10^{-5} and with the limit on total channel iterations being 1, 2, or 3, the average number of channel iterations is 1, 1.2 and 1.5 respectively. The average number of LDPC iterations under these conditions is about 5, 20 and 35 respectively. From Fig. 3, it can be seen that at bit error rate 10^{-5} , the gain for a maximum of 3 channel iterations is about 0.3 dB over a single channel iteration or in other words no turbo equalization, but it takes a factor of seven increase in total number of LDPC iterations.

V. LDPC CODE DESIGN ALGORITHM

We wanted an LDPC code to be long enough to hold a standard 4096-bit disk sector after passing through the rate 16/17 QMTR encoder and with a code rate around 0.94.

Any parity check matrix \mathbf{H} can be thought of as a many-to-many mapping from codeword bits to parity checks and vice versa [14]. If we create a set $B = \{b_0, b_0, b_0, b_1, b_1, b_1, \dots\}$ of the codeword bits, with each bit b_i appearing in the set a number of times equal to the weight of that column of \mathbf{H} , and a similar set $C = \{c_0, c_0, \dots, c_1, c_1, \dots\}$ of the parity checks, then any parity check matrix \mathbf{H} corresponds to some permutation \mathbf{S} from elements of B to elements of C . The goal is to find a mapping \mathbf{S} that leads to an LDPC code matrix \mathbf{H} such that the resulting code has no 4-cycles. It has been found that 4-cycles are detrimental to the bit error rate performance of LDPC codes [6].

The code design algorithm is as follows:

1. Compute the desired codeword size N and number of parity checks M and randomly generate a permutation \mathbf{S} of the desired size (the total number of ones in \mathbf{H}).
2. Check \mathbf{S} to see that it corresponds to a valid \mathbf{H} matrix. If we find that \mathbf{S} is mapping the bit b_i to a check c_j more than once, we randomly swap the target of that one mapping with some other mapping in \mathbf{S} and repeat until we get a suitable \mathbf{S} .
3. Check the permutation for 4-cycles. If we find none, we proceed to Step 5.
4. If we did find a 4-cycle involving some codeword bit b_i , we randomly pick another codeword bit b_j and exchange the targets of the two checks that \mathbf{S} maps these two bits to and go back to Step 2.
5. Now we have an \mathbf{S} corresponding to a cycle-free \mathbf{H} , the final stage is to reorder the columns such that the right-most $M \times M$ section is invertible and \mathbf{H} can be converted to a generator matrix.

Whether this algorithm converges in any given situation is by no means obvious. In practice, it appears that the algorithm converges much less rapidly with attempts to create codes of rates much above 0.95, codes of very short length, and codes with column weight larger than three.

VI. CONCLUSION

A serially concatenated system using our LDPC code and iterative decoding has been introduced for use on a ME²PR4-equalized Lorentzian channel. Simulation results show that a gain of 5.9 dB over uncoded EPR4 at a bit error rate of 10^{-5} can be obtained. These significant gains make LDPC coded systems very attractive as an alternative to turbo coded magnetic recording systems. Although this work was done independently of Fan *et al.* [15], the authors were recently made aware of their work on the performance of an LDPC coded system for an ideally equalized EPR4 channel.

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