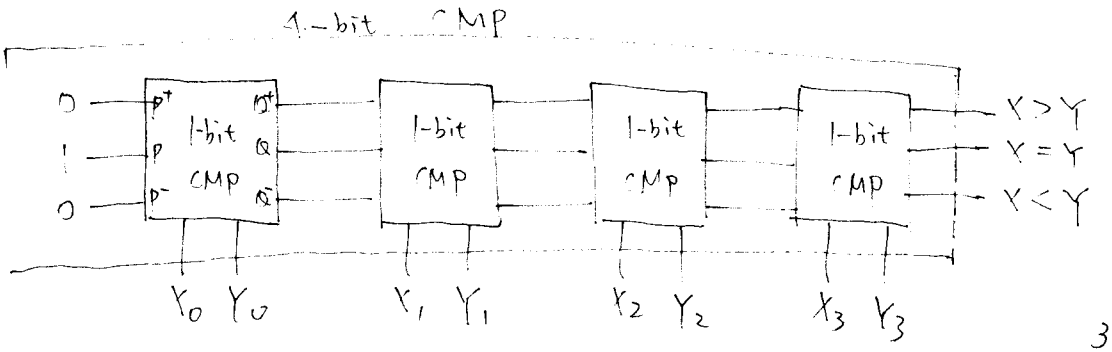
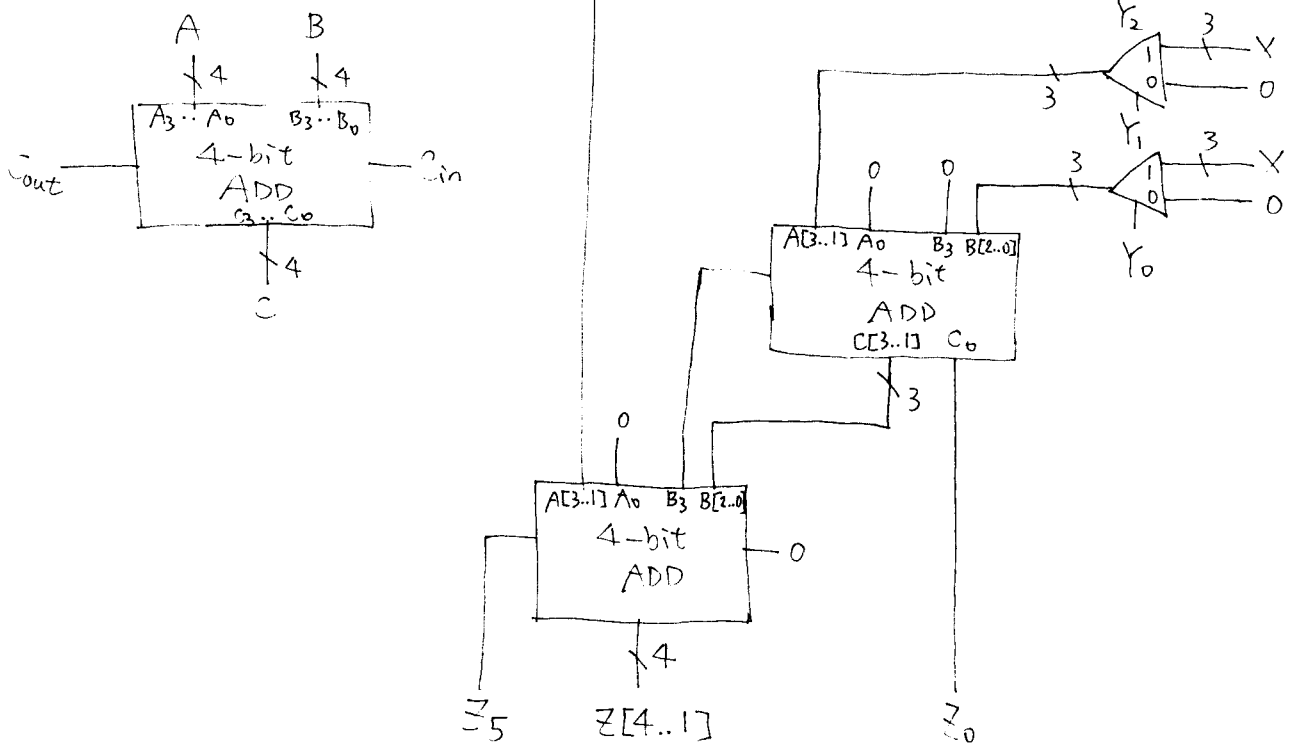


7.



8.

	MUX_A	MUX_B	MUX_C	MUX_D	MUX_E	REG_W	MEM_W	ALU_{OP}
sub	*	*	1	0	00	1	0	000
ld	*	0	*	1	10	1	0	*
jr	0	*	*	0	*	0	0	100