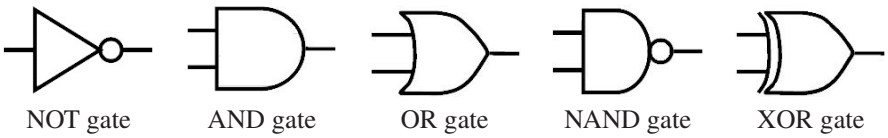
922 25300 Computer Organization and Assembly Languages | **National Taiwan University**
Fall 2007 | **Department of CSIE**

Homework 1

October 8, 2007 | Due date: October 22, 2007

- *Signed integers are represented using two's complement representation.*
- *Please use the following notations for logic gates. Feel free to change the orientations of the gates and the positions of inputs and outputs. You are free to use other circuits. However, if they are not introduced in the class, you have to implement them before using them.*



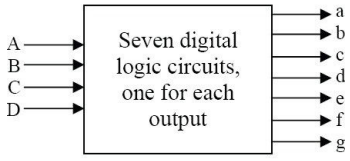
NOT gate AND gate OR gate NAND gate XOR gate

1. (10%) What are the 8-bit binary representations of the following signed decimal integers? Convert them into hexadecimal.
   a. 51
   b. -5

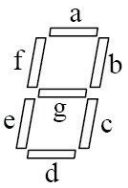
2. (10%) Prove that (a) {NOT, OR} and (b) {NAND} are universal.

3. (10%) (a) Create the truth table for the 3-input Boolean function, Even, which returns 1 if the number of zeros in inputs is even, 0 otherwise. (b) Implement this function with logic gates AND, OR and NOT.

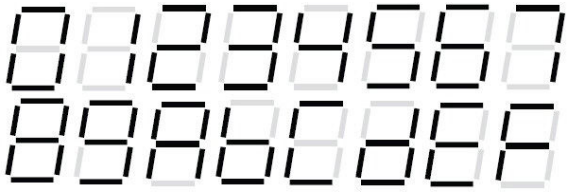
4. (20%) Follow the conventions in the following figure. Design a 7-segment display driver which accepts a 4-bit input (ABCD where A is the MSB) and outputs 7 bits which controls the on/off status of a 7-segment display as shown in the above figure. (a) List the truth table for the driver. (b) Write down the Boolean expressions for segments a and e.



(a) 7-segment display driver

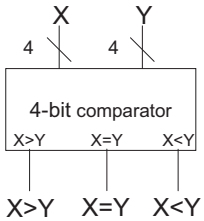


(b) names of segments



(c) Configurations for 16 hexadecimal digits

5. (15%) As shown in the following diagram, design a 4-bit comparator which has two 4-bit unsigned integer inputs, $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$, and a 3-bit output for the conditions of $X > Y$, $X = Y$ and $X < Y$, respectively. *Hint: design a 1-bit comparator first.*



6. (20%) Design a binary multiplier that multiplies two 3-bit unsigned integers, $X = X_2X_1X_0$ and $Y = Y_2Y_1Y_0$, and a 6-bit output $Z = Z_5Z_4 \ldots Z_0$ and $Z = X \times Y$, where X_0, Y_0 and Z_0 are LSBs. You may use the notation $X[n..m]$ to identify a portion of wires. For example, X[2..1] means the set of wires, X_2X_1.

7. (15%) Refer to the following figure for TOY architecture. Please specify the operations of MUX_A, MUX_B, MUX_C, MUX_D, MUX_E, REG_W, MEM_W and ALU_{OP} during the execution stage for the instructions "load address", "store indirect" and "branch zero". For example, the answer for "jump and link" would be $MUX_A = 0, MUX_B = *, MUX_C = *, MUX_D = 1, MUX_E = 01, REG_W = 1, MEM_W = 0, ALU_{OP} = *$.