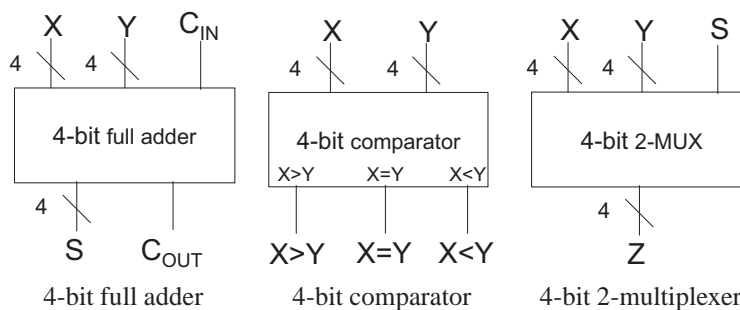
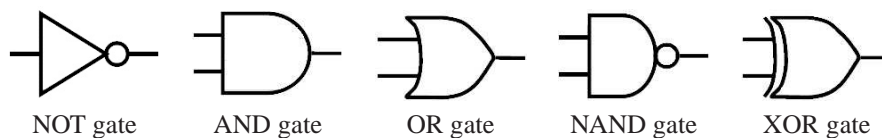


## Homework 1

October 2, 2006

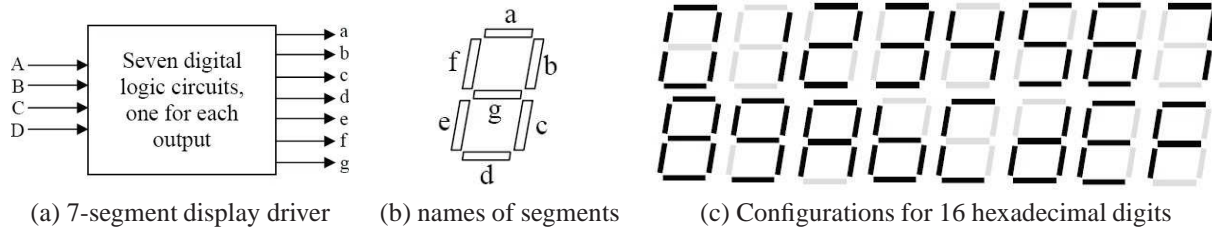
Due date: October 16, 2006

- Signed integers are represented using two's complement representation.
- Please use the following notations for logic gates. Feel free to change the orientations of the gates and the positions of inputs and outputs. You are free to use other circuits. However, if they are not introduced in the class, you have to implement them before using them.

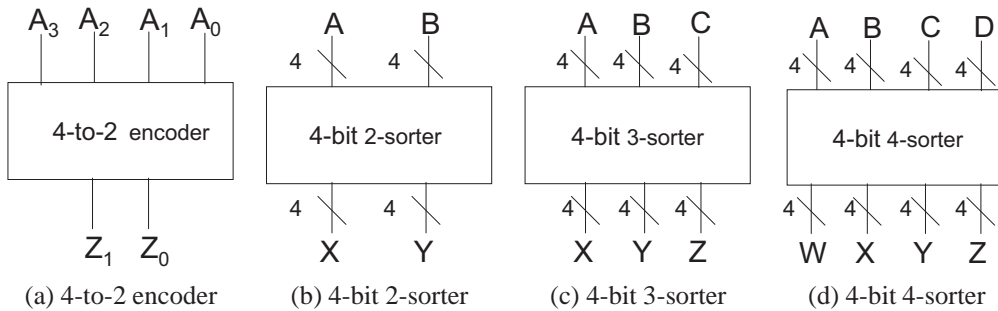


- (6%) What are the decimal and the hexadecimal representations of each of the following unsigned binary integers?
  - 01010110
  - 10011100
  - 11101010
- (6%) What are the binary representations of the following hexadecimal numbers? What are the decimal numbers they represent when interpreted as 8-bit unsigned and signed integers respectively?
  - 5A
  - CB
- (6%) What are the 8-bit binary representations of the following signed decimal integers?
  - 12
  - 97
- (8%) What is the sum of each pair of signed binary integers? Perform the addition using the binary number system and show the process. Verify your answer using the decimal number system.
  - 01001100 + 00001111
  - 01010101 + 11101011
- (10%) Convert the 32-bit single-precision IEEE 754 numbers shown below into real numbers in decimal system.
  - 40D40000
  - BEC00000

6. (10%) Convert the following numbers into 32-bit single-precision IEEE 754 numbers. Display them in the hexadecimal format.
- $9.25_{10}$
  - $1.0101_2 \times 2^{-130}$
7. (6%) Prove that (a) {NOT, AND} and (b) {NOR} are universal.
8. (12%) (a) Create the truth table for the Boolean function  $Z = A\bar{B} + \bar{B}C$  (4%). (b) Implement this function with logic gates AND, OR and NOT (4%). (c) Use only NOR gates to implement this function (4%).



9. (16%) Design a 7-segment display driver which accepts a 4-bit input (ABCD where A is the MSB) and outputs 7 bits which controls the on/off status of a 7-segment display as shown in the above figure. (a) List the truth table for the driver. (b) Write down the Boolean expressions for segments a and e.



10. (8%) A 4-to-2 encoder (Figure (a)) has four inputs  $A_3, A_2, A_1, A_0$  and two outputs  $Z_1, Z_0$ . Only one of the four inputs can be 1 at a time. Assume that  $A_i$  is on, the output  $(Z_1, Z_0)$  will correspond to the binary representation of  $i$ . For example, when input  $A_2=1$ ,  $(Z_1, Z_0)=(1,0)$  because  $10_2 = 2_{10}$ . Create the truth table for the 4-to-2 encoder and implement it with logic gates.
11. (12%) (a) A 4-bit 2-sorter (Figure (b)) has two 4-bit inputs A, B and two 4-bit outputs X, Y. The inputs A and B are unsigned integers. The output X is the larger one of A and B and Y is the smaller one of A and B. Design a 4-bit 2-sorter using the components introduced in the class. [Hint: one possibility is to composite 4-bit comparators and 4-bit 2-multiplexers to complete the task.] (b) A 4-bit 3-sorter (Figure (c)) has three 4-bit inputs A, B, C and three 4-bit outputs X, Y, Z, where X, Y and Z are the result of sorting A, B, C so that  $X \geq Y \geq Z$ . Use 4-bit 2-sorters to composite a 4-bit 3-sorter. (c) A 4-bit 4-sorter (Figure (d)) has four 4-bit inputs A, B, C, D and four 4-bit outputs W, X, Y, Z with  $W \geq X \geq Y \geq Z$ . Design a 4-bit 4-sorter.