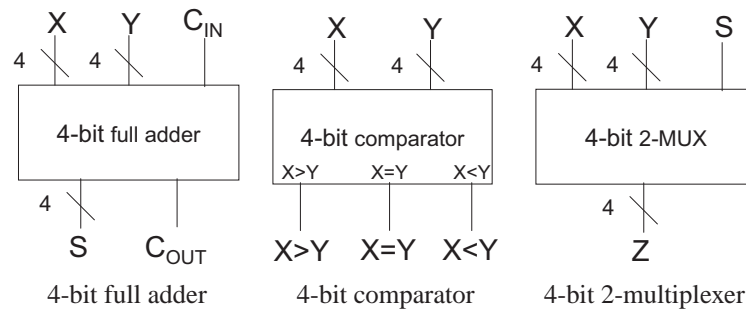
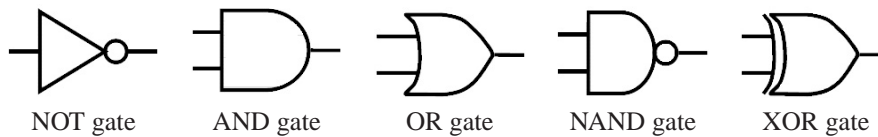


Homework 1

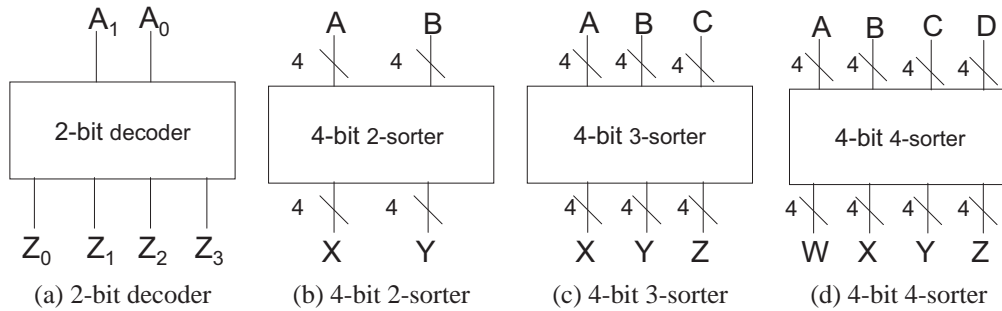
October 13, 2005

Due date: October 27, 2005

- Signed integers are represented using two's complement representation.
- Please use the following notations for logic gates. Feel free to change the orientations of the gates and the positions of inputs and outputs. You are free to use other circuits. However, if they are not introduced in the class, you have to implement them before using them.



- (6%) What are the decimal and the hexadecimal representations of each of the following unsigned binary integers?
 - 10101000
 - 01001100
 - 00110101
- (6%) What is the binary representation of the following hexadecimal numbers? What are the decimal numbers they represent when interpreted as unsigned and signed integers.
 - B4A7
 - 1F6E
- (8%) What is the sum of each pair of signed binary integers? Perform the addition using the binary number system and show the process. Verify your answer using the decimal number system.
 - 00110101 + 00001111
 - 11010101 + 01101011
- (4%) What is the 8-bit binary representation of the following signed decimal integers?
 - 16
 - 94
- (10%) (a) Design a circuit to perform two's complement operation for a 4-bit binary number (7%). (b) Combined with 4-bit full-adder, design a 4-bit subtractor (3%).
- (8%) (a) Create the truth table for the Boolean function $Z=A+BC$ (2%). (b) Implement this function with logic gates AND, OR and NOT (2%). (c) Use only NAND gates to implement this function (4%). [Hint: use DeMorgan's law $((X + Y)' = X'Y'$ and $(XY)' = X' + Y'$.]



7. (10%) A 2-bit decoder (Figure (a)) has two inputs A_1, A_0 and four outputs Z_0, Z_1, Z_2 and Z_3 . Given an assignment of the input Boolean variables (A_1, A_0), the output corresponding to the binary representation of (A_1, A_0) will be 1, the others will be 0. For example, when input (A_1, A_0)=10, Z_2 is 1 because binary 10 represents decimal 2. Create the truth table for the 2-bit decoder and implement it with logic gates.
8. (12%) (a) A 4-bit 2-sorter (Figure (b)) has two 4-bit inputs A, B and two 4-bit outputs X, Y . The inputs A and B are unsigned integers. The output X is the larger one of A and B and Y is the smaller one of A and B . Design a 4-bit 2-sorter using the components introduced in the class. [Hint: one possibility is to composite 4-bit comparators and 4-bit 2-multiplexers to complete the task.] (b) A 4-bit 3-sorter (Figure (c)) has three 4-bit inputs A, B, C and three 4-bit outputs X, Y, Z , where X, Y and Z are the result of sorting A, B, C so that $X \geq Y \geq Z$. Use 4-bit 2-sorters to composite a 4-bit 3-sorter. (c) A 4-bit 4-sorter (Figure (d)) has four 4-bit inputs A, B, C, D and four 4-bit outputs W, X, Y, Z with $W \geq X \geq Y \geq Z$. Design a 4-bit 4-sorter.
9. (12%) What are the control signals of the instructions SUB, JE, STA and CMP for the toy machine we introduced in the class? Use the notation we used in the class. For example, the control signals for JG are (1) IR_{RD} , $FLAG_{RD}$ and (2) $FLAG_{01}$.
10. (12%) Convert the following assembly code into machine code as we did in the class. Draw the memory layout and the content after the program is loaded. Write down contents of the registers PC, IR, ACC, B and FLAG(NGEL) after executing each instruction.

```

.DATA
A      007
B      002
C      009
ONE    001
.CODE
      LDA  A
      CMP  B
      JG   L1
      JMP  END
L1    CMP  C
      JG   L2
      JMP  END
L2    ADD  ONE
      STA  A
      END  HLT

```

11. (12%) Write an assembly program for our toy machine which accepts two unsigned integers A and B ($A < B$) and ACC holds $\lceil \frac{A+B}{2} \rceil$ when the program halts. Note that $\lceil x \rceil$ is the ceiling operation which returns the smallest integer that is larger than or equal to x . For example, $\lceil 3.5 \rceil = 4$.